What Is Claimed Is:

A method for transmitting a control signal to an option pad of an 1. integrated circuit chip at its package level comprising the steps of:

electrically isolating one of a plurality of commonly connected power transmitting pins of the integrated circuit package;

connecting the electrically isolated power transmitting pin to the option pad to thereby transmit a control signal from outside through the electrically isolated power transmitting pin to the option pad.

- The method, as defined in claim 1, wherein the commonly connected 2. power transmitting pins is connected to ground.
- The method, as defined in claim 1, wherein the commonly connected 3. power transmitting pins is connected to a power supply.
- The method, as defined in claim 1, wherein the option pad is a pad for 4. performing a burn-in test at the package level.
- 5. The method as defined in claim 1, wherein the control signal is an external signal to perform a burn-in test at the package level.
- 6. The method, as defined in claim 1, wherein the control signal is an external signal to perform one of burn-in test, input/output test, and parallel bit test.

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- 7. The method, as defined in claim 1, wherein the integrated circuit package includes a ball grid array pin arrangement.
- 8. The method, as defined in claim 1, wherein the integrated circuit chip includes a static random access memory device.
- 9. An integrated circuit package having an integrated circuit chip for transmitting a test control signal from outside, comprising:

the integrated circuit chip being mounted in the integrated circuit package with power pads connected with an option pad and power lines connected to an internal circuit;

power transmitting group pins connected to the power pads of a plurality of power transmitting pins assigned and formed at the integrated circuit package; and

at least one signal transmitting pin connected to the option pad but electrically isolated from the power transmitting group pins.

- 10. The structure, as defined in claim 9, wherein the power pads are ground voltage pads when the power transmitting pins are ground voltage pins.
- 11. The structure, as defined in claim 9, wherein the power pads are power supply voltage pads when the power transmitting group pins are supply power voltage pins.
- The structure, as defined in claim 9, wherein the option pad is a pad for performing a burn-in test at the package level.

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- 13. The structure, as defined in claim 9, wherein the control signal is an external signal to perform a burn-in test at the package level.
- 14. The structure, as defined in claim 9, wherein the control signal is an external signal to perform one of burn-in test, input/output test, and parallel bit test.
- 15. The structure, as defined in claim 9, wherein the integrated circuit package includes a ball grid array pin arrangement.
- 16. The structure, as defined in claim 9, wherein the integrated circuit chip includes a static random access memory device.
- 17. The structure, as defined in claim 9, wherein the option pad includes an electric static discharge circuit.
- 18. The structure, as defined in claim 9, wherein the option pad includes a keeper circuit to prevent a false operation of a device when the signal transmitting pin is open.
- The structure, as defined in claim 9, wherein the internal circuit is constructed with an option receiver having an inverter structure.

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20. A method for performing a test by controlling an internal circuit of a package chip at the package level, comprising the steps of:

connecting a power transmitting pin to an option pad, the option pad being accessible only at the wafer level;

isolating the power transmitting pin from a plurality of power transmitting pins commonly connected to one of power and ground; and

transmitting a test control signal to the option pad through the power transmitting pin.

